

Integrated Second-Stage Power IC for Two-Stage 12-Switch ZIV Converter with On-Chip Precharge Scheme for Vertical Power Delivery

Cheng-Ta Chuang

Graduate Institute of Electrical Engineering
National Taiwan University
Taipei, Taiwan
darcyboogi286@gmail.com

Ching-Jan Chen

Graduate Institute of Electrical Engineering
National Taiwan University
Taipei, Taiwan
chenjim@ntu.edu.tw

Yan-Fei Liu

Department of Electrical and Computer
Engineering
Queen's University
Kingston, Canada
yanfei.liu@queensu.ca

Abstract—The proliferation of AI workloads in laptop CPUs and GPUs necessitates high current to sustain peak performance. To mitigate conduction losses, vertical power delivery (VPD) has become a critical requirement; however, conventional architectures remain constrained by bulky inductors with high package height. This paper presents a design of two-stage 12-switch Zero-Inductor-Voltage (ZIV) converter for 5 V-to-1.25 V conversion with a scalable output current of up to 2 A. The proposed converter includes a discrete first stage and two versions of second-stage power ICs with integrated pre-charge control in TSMC 0.18- μm HV BCD technology to mitigate inrush current and reduce board area. One implementation uses conventional die pads and wire bonds to connect the power IC to the printed circuit board (PCB). The other implementation utilizes through-silicon via (TSV) and metal bumps to connect the main power rail of the power IC to the PCB. Operating at 2 MHz, the architecture only requires two selected 15 nH inductors to maintain the dominant component height within 0.6 mm, offering a scalable solution suited for VPD applications.

Keywords—Zero-Inductor-Voltage Converter (ZIV), low inductance, power IC, vertical power delivery

I. INTRODUCTION

The scaling of AI-enabled mobile processors in portable devices like laptops and smartphones is pushing CPUs and GPUs toward lower supply voltages and higher current levels. This trend increases conduction losses in the power-delivery network (PDN), as a larger current must flow through interconnects between the converter and the load. To mitigate these losses, next-generation systems are trending toward vertical power delivery (VPD) [1], which places the converters and passives directly beneath the load processor package to minimize parasitic impedance and shorten the conduction path. Additionally, conventional point-of-load (PoL) converters are widely used to supply low voltages and high current to processors, but their implementations are often limited by the size of passive components because of the topology requirement. In particular, prior PoL solutions targeting VPD or high-performance computing platforms [2]-[8] typically adopt topologies and rely on relatively large inductors to suppress output current ripple. These inductors are typically realized by discrete components, which occupy considerable board area and

increase total system height. Prior VPD demonstrations, such as [1], have integrated the load and power-management ICs within the same package, yet the discrete inductor still occupies significant volume relative to the packaged power IC, limiting the system's compactness. Other works have proposed custom inductor structures to reduce inductor volume. [9]-[11] utilized customized inductors to form a scalable VPD module. However, such customization requires additional fabrication processes and introduces manufacturing challenges. [12] and [13] proposed novel architectures and chiplets to integrate high-voltage converters within a small form including inductors and capacitors, but also remains reliance on specific process and integration techniques.

In contrast, the Zero-Inductor-Voltage (ZIV) converter family [14], [15] shapes the inductor voltage to near zero under steady-state operation, enabling the use of substantially smaller inductance without additional specialized inductor design, thereby reducing the total system size. The goal of inserting an inductor into a power converter is to keep the output current continuous. However, the inductor results in current ripple from the voltage across the inductor, as expressed in (1) and (2)

$$V_L = L \frac{dI_L}{dt} \quad (1)$$

$$\frac{dI_L}{dt} = \frac{1}{L} V_L \quad (2)$$

Generally, many prior works focus on increasing inductance to suppress the output current ripple, but this follows by large inductor packaging and footprint. The ZIV converter derives from the idea of decreasing the voltage across the inductor to further reduce the inductance the converter requires. The original ZIV converter employs seven switches, as shown in Fig. 1. By driving complementary switch pairs with appropriate timing, the inductor experiences an approximately zero average voltage, allowing a much smaller inductor than that required in conventional topologies. Based on this principle, several ZIV-family converter topologies have been developed, including topologies that parallel the output paths [15] and approaches that

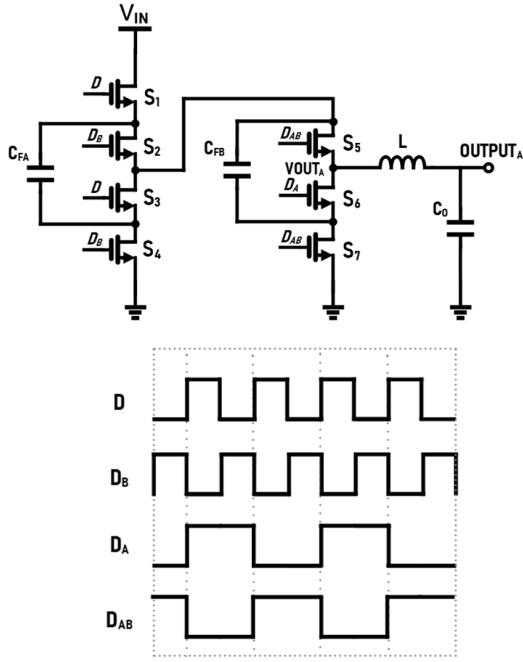


Fig. 1. Topology of 7-switch ZIV converter and switch operation waveform

extend the effective conversion ratio range [16]. These developments highlight the scalability and potential of the ZIV converter family for high-current applications and are attractive for VPD implementations.

Prior works on ZIV converters target high-voltage applications in data centers that require 48 V to 12 V; thus, they mainly rely on the robustness of the discrete devices to withstand the high voltage across the devices and startup inrush conditions. This work extends the open-loop 12-switch ZIV converter concept toward PoL applications through partially chip-scale implementation and proposes a two-stage system architecture for the converter. Moreover, this work implements an additional chip version to realize the proposed two-stage 12-switch ZIV converter in a VPD network.

This paper is organized as follows. Section II first describes the 12-switch ZIV converter and introduces the proposed two-stage system with two implementation methods in the work. Section III presents the proposed on-chip precharge scheme for the chip and details the key sub-circuit blocks in the integrated second-stage chip. In Section IV, the specifications and simulation results are shown. Finally, Section V concludes the paper and discusses the future work.

II. 12-SWITCH ZERO-INDUCTOR-VOLTAGE CONVERTER AND PROPOSED TWO-STAGE SYSTEM

A. 12-Switch Zero-Inductor-Voltage Converter

Derived from the original 7-switch ZIV converter, the 12-switch ZIV topology also achieves low inductance by utilizing flying capacitors to shape the inductor voltage so it remains near zero in steady state [13]. Fig. 2 shows the topology of the 12-switch ZIV converter. The topology parallels the output path of

the 7-switch ZIV converter and removes two redundant power MOSFETs. The converter sequentially cycles through the four operating states illustrated in Fig. 2. The switches are driven by complementary gate signals with a fixed 50% duty cycle, ensuring that the voltages at the switching nodes, VOUT1 and VOUT2, inherently settle at $0.25V_{IN}$. Thus, the voltage drop across the inductor is theoretically near zero during steady-state operation, permitting the use of a small 15-nH inductor. Moreover, the 12-switch topology increases switch utilization relative to the 7-switch topology converter and thus reduces the RMS current flowing through power MOSFETs in the first stage, which reduces conduction loss significantly.

B. Proposed Two-Stage System

Prior works implement the ZIV converter family with commercial discrete devices with large footprints. This work aims to realize a 12-switch ZIV converter at chip scale and broaden the application of the ZIV converter to portable computing systems like laptops and cellphones. However, implementing a full 12-switch ZIV converter at chip scale concentrating all power devices on a single die increases the risk of yield loss and single-point failure due to process-related defects. A failure in any one of the integrated power switches can affect the entire converter. Therefore, this work partitions the converter into two stages to improve system robustness. The first stage is implemented by carefully selected discrete devices,

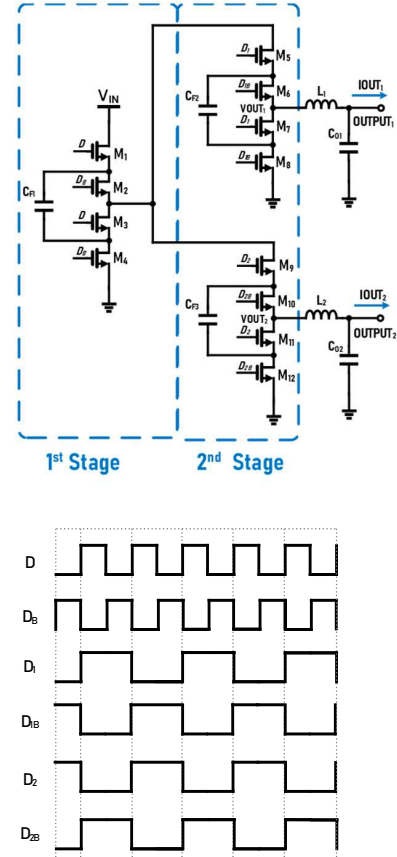


Fig. 2. Topology of 12-switch ZIV converter and switch operation waveform

while the second stage includes two identical ICs connected in parallel to enhance total system yield and future scalability. Each IC integrates four power MOSFETs and the required supporting sub-circuits, including gate drivers, a frequency divider, a constant-gm current source, a non-overlap circuit, and the proposed capacitor pre-charging circuits. The capacitors and inductors are implemented by discrete components. Fig. 3 illustrates the proposed two-stage 12-switch ZIV converter system. A jumper is included between the first stage and the second stage to enable flexible measurements of each stage independently or the full system.

As AI workloads continue to increase the current demand, power delivery losses on board interconnect have become a challenge to increasing efficiency. VPD is therefore gaining attention because it shortens the power path and reduces conduction loss associated with long planar routing. In addition, the ZIV converter family relaxes the inductance requirement by minimizing the dc voltage stress across the output inductor under steady-state operation, enabling the use of very small inductors. This characteristic is well aligned with VPD integration, as the inductor profile can be reduced and may be further co-packaged with, or integrated into, the power IC to decrease the overall volume and z-axis height. This work leverages advanced packaging technology to realize an architecture compatible with VPD of the proposed system to further improve the system efficiency. Fig. 4 compares the two architectures implemented in this work. Fig. 4(a) shows the conventional planar power delivery network that connects the dies to the PCB through bonding wires, while Fig. 4(b) indicates the VPD implementation. In the VPD implementation, the power IC functions as an active interposer with through-silicon vias (TSVs) [17], [18]. With the TSVs, the load chip can be stacked vertically on the interposer, resulting in much shorter distances between the converter and the load. Moreover, metal bumps are used between the interposer and the PCB, which further removes the bonding wires that lead to resistive loss and parasitic inductance.

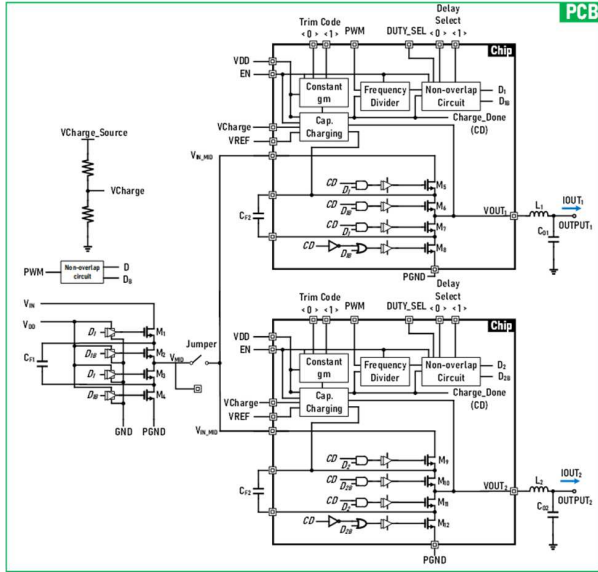


Fig. 3. Proposed two-stage 12-switch ZIV converter system

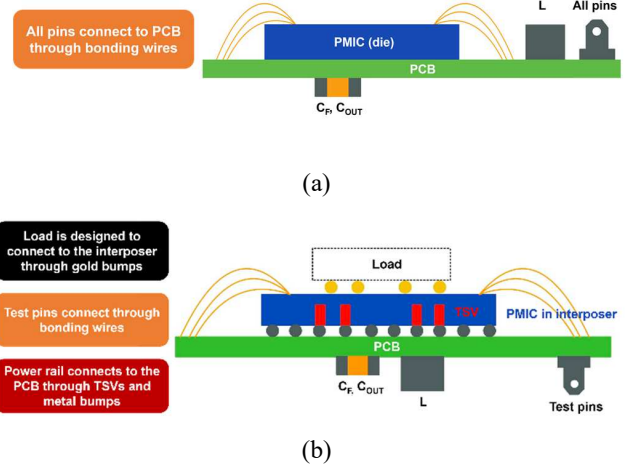


Fig. 4. (a) Conventional planar power delivery network implementation (b) Vertical power delivery implementation

III. PROPOSED PRE-CHARGING SCHEME AND CIRCUIT IMPLEMENTATION

A. Proposed Pre-Charging Architecture

Fig. 5 illustrates the architecture of the proposed pre-charging scheme. During startup, two key nodes CF_P and $VOUT_1$ must be charged up to their target voltage to avoid the high inrush current when the main power stage starts operating. Otherwise, the input voltage will be connected to the positive node of the flying capacitor and the large voltage change will result in high inrush current. Both nodes are charged using similar precharge circuits. For the positive node of the flying capacitor CF_P , the comparator compares the voltage with an external reference voltage $VREF$. While V_{CF_P} remains below $VREF$, the comparator output remains high and forces the D flip-flop complementary output to a high state (5V). Thereby, turning on the charging switch M_{Charge_CF} . During pre-charging, the power MOSFET M8 is also turned on to provide a charging path to ground. Once the voltage of the node CF_P reaches $VREF$, the output of the comparator becomes zero and raises the clock input of the D flip-flop to pass the high signal from D to Q. Thus, the CF_Done signal will be pulled high to indicate the precharging of CF_P is complete and disables both M_{Charge_CF} and the comparator. The pre-charging scheme of $VOUT$ is also designed as the same mechanism, except no additional switch has to be turned on to provide a path to ground. After both nodes have been precharged, $Charge_Done$ will be pulled high to enable the subsequent blocks and the converter transitions to normal operation.

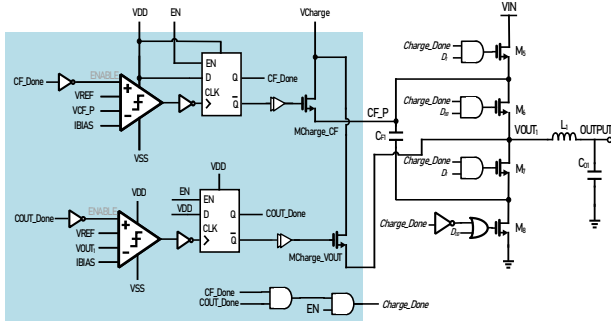


Fig. 5. Proposed pre-charging circuit

B. Frequency Divider

As discussed in Section II, the operating principle can be interpreted as two complementary signals in each stage. The switching frequency of first-stage is twice that of the second stage. Since there will be one single pulse input in system level, an on-chip frequency divider is required and shown in Fig. 6. The frequency divider takes the pulse from the system level and outputs a pulse signal at half the input frequency. Particularly, a 2-MHz system clock directly drives the first stage and is divided by two on-chip, resulting in a 1-MHz switching frequency for each second-stage IC. Moreover, a multiplexer controlled by the select pin DUTY_SEL is used to choose the polarity of the output pulse, ensuring the paralleled chips in the second stage work in an interleaved manner.

C. Non-overlap circuit

The non-overlap circuit shown in Fig. 7 provides an adjustable dead time to prevent shoot-through during switching transitions. In each stage, the power switches are controlled by two interleaved pulse signals with 50% duty cycle. To prevent simultaneous conduction of the four power MOSFETs in each chip and the resulting shoot-through current, the non-overlap circuit is designed to create dead-time between two pulse signals. Moreover, in practical implementations, parasitic resistance and capacitance along the signal paths can further slow signal edges and alter the overlap margin. To compensate for the undesirable condition, a tunable dead-time trim is included before the pulse signals are delivered to the gate drivers. In this work, the non-overlap function is realized with discrete components in the first stage, while it is integrated on-chip for the second stage.

IV. CHIP IMPLEMENTATION AND SIMULATION RESULTS

The proposed designs demonstrate high efficiency and improved robustness based on the simulation results. Table I summarizes the simulation setup and key specifications. Fig. 8 presents the steady-state operating waveform of the proposed system, and Fig. 9 illustrates the startup waveform from power-up to steady-state operation and shows that the proposed precharge circuit suppresses inrush current and output voltage overshoot, both of which can otherwise introduce malfunction risk to the integrated circuit. Upon enablement at t1, the flying capacitor node CF_P and VOUT ramp up without risky

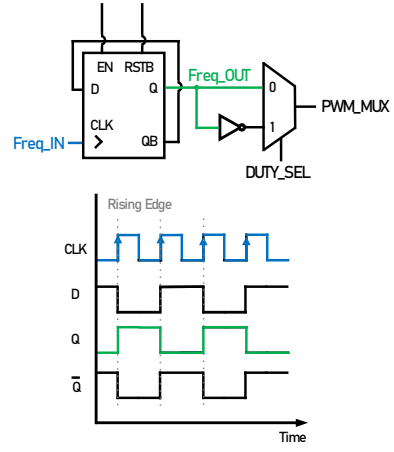


Fig. 6. Frequency divider and polarity select

overshoot and inrush current. A verification window from t2 to t3 confirms the successful deactivation of the pre-charge path before the main power stage initiates at t3. The efficiency simulations are being conducted for two configurations: a wire-bonded implantation and a VPD implementation. Although the VPD version incorporates TSVs and supports stacking a load chip onto the power converter through gold bumps directly, this work focuses on the implementation of the power converter itself, utilizing pins and pads on the PCB to measure performance rather than an additional stacked load chip. The chip efficiency and the system efficiency is defined as (3) and (4).

$$\eta_{chip} = \frac{P_{OUT_chip}}{P_{IN_chip}} \quad (3)$$

$$\eta_{system} = \frac{P_{OUT}}{P_{IN}} \quad (4)$$

P_{IN_chip} is the input power tested from the PCB pad that connects to the input pad of the chip, and P_{OUT_chip} is the power tested from the PCB pad connected to the chip output. P_{IN} defines the input power from the voltage source and P_{OUT} is tested from the same point as P_{OUT_chip} . The simulation of the version of conventional planar power delivery includes the bonding wires between the chips and the PCB. On the other hand, the chip efficiency of the version with VPD design is simulated by removing the bonding wires on the main power rail to model the actual implementation. Fig. 10 shows that the design reaches peak chip efficiency 94.03% and 96.8% among the two versions. The figure shows the efficiency is much improved especially when load current increases, which results from the removal of bonding wires connecting to the PCB that possess large parasitic resistance. Fig. 11 shows the simulation results of efficiency changes of the full power converter system to changes of the load current. The conduction loss of the first stage is simulated according to the designed PCB and reaches peak efficiency of 95.1% with vertical power delivery configuration. Fig. 12 includes the layouts and descriptions of the two versions of the chip implementations designed in a TSMC 0.18- μ m high-voltage

BCD process. Two layouts occupy active areas of $4.612 \text{ mm} \times 2.032 \text{ mm}$ and $4.721 \text{ mm} \times 2.032 \text{ mm}$, respectively. Fig. 13 is the PCB design and will be used to measure the actual system performance and metal bumps effectiveness after fabrication is completed.

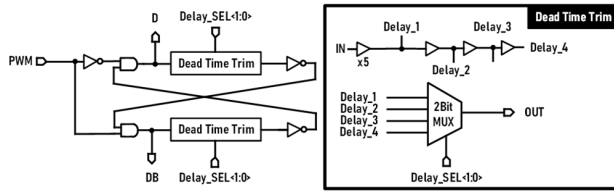


Fig. 7. Non-overlap circuit

TABLE I. KEY PARAMETERS

Parameter	Value	
System input voltage	5 V	
Output voltage	1.25 V	
Load current	1 A (per output path)	
Switching frequency (1 st stage)	2 MHz	
Switching frequency (2 nd stage)	1 MHz	
M1 ~ M4 R_{on}	20 m Ω (simulation)	
M5 ~ M12 R_{on}	20 m Ω (post-layout simulation)	
L_1, L_2	15 nH 0402 package $1 \text{ mm} \times 0.5 \text{ mm} \times 0.35 \text{ mm}$	
C_{F1}, C_{F2}, C_{F3}	$1 \mu\text{F} \times 2$ Murata Electronics GRM152R60J105ME15D	
C_{OUT}	$10 \mu\text{F} \times 2$ Murata Electronics GRM155R60J106ME47D	
Resistance per bonding wire	10 m Ω	
Inductance per bonding wire	10 nH	
Capacitance per bonding wire	600 fF	
Main power MOSFET size (M5 ~ M12)	$1.935 \text{ mm} \times 1.138 \text{ mm}$	
Chip efficiency simulation (planar power delivery)	Peak 94.03% (at 400 mA)	92.2% (at 1 A)
Chip efficiency simulation (vertical power delivery)	Peak 96.8% (at 800 mA)	96.6% (at 1 A)
System efficiency simulation (planar power delivery)	Peak 94.4% (at 300 mA)	90.2% (at 1 A)
System efficiency simulation (vertical power delivery)	Peak 95.1% (at 800 mA)	95.0% (at 1 A)

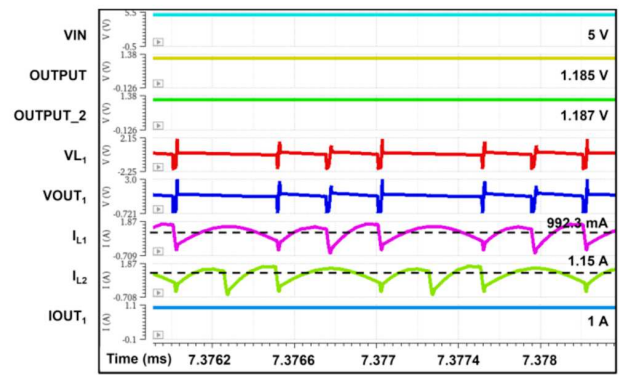


Fig. 8. Simulation result of steady-state operation under 1 A load per chip waveform

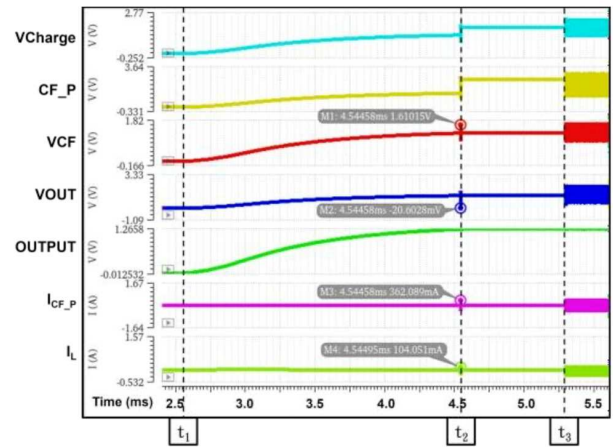


Fig. 9. Simulated startup waveforms with the proposed precharge circuits.

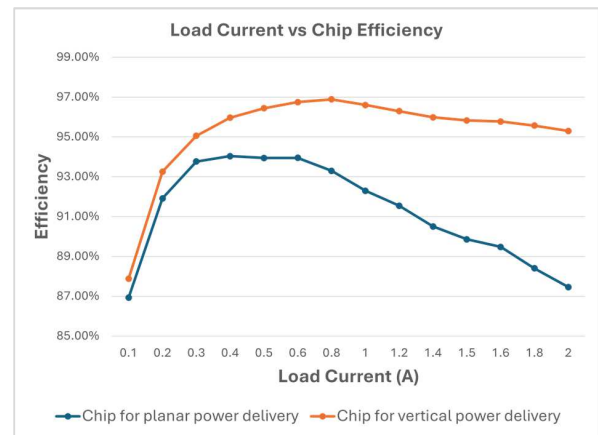


Fig. 10. Simulation result of chip efficiency vs load current.

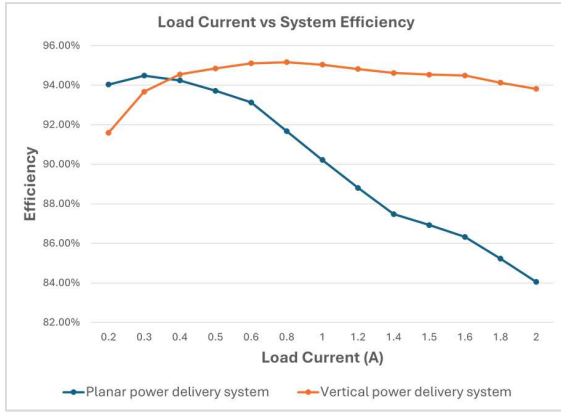


Fig. 11. Simulation result of system efficiency vs load current

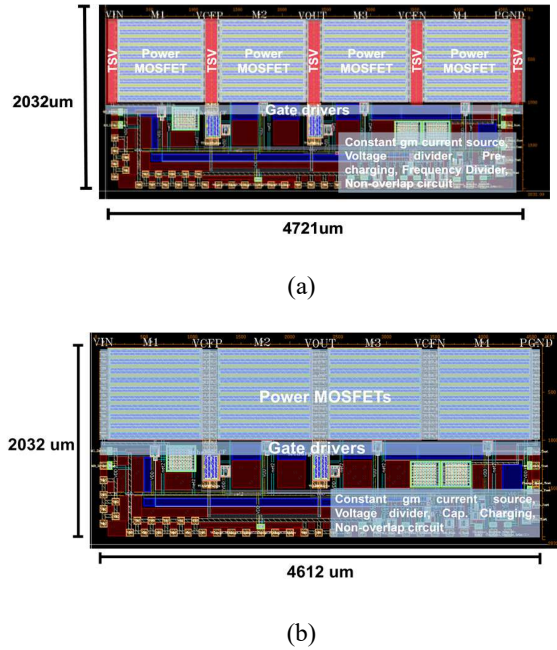


Fig. 12. (a) Chip layout for conventional planar power delivery (b) Chip layout for vertical power delivery

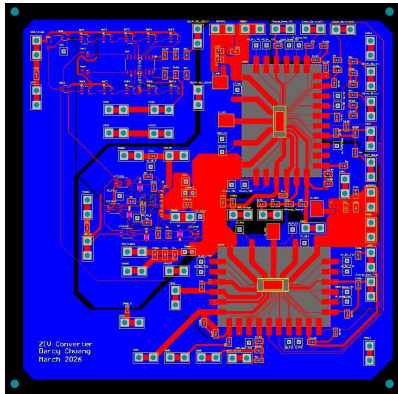


Fig. 13. PCB design for proposed two-stage 12-switch ZIV converter

V. CONCLUSION

This paper presents two implementations of an open-loop two-stage ZIV converter with integrated second-stage power ICs. The first implementation uses conventional wire bonds to connect the power ICs to the PCB, whereas the second implementation uses TSVs and metal bumps to realize a VPD structure by fabricating the ICs in the interposer without wire bonds in the main power rail. At 1 A per output path, the simulated system efficiencies are 90.2% and 95.0% for the planar and VPD implementations, respectively. The improved efficiency of the VPD implementation mainly results from the reduced parasitic resistance in the main power path. The small 15-nH inductance helps minimize the overall converter volume and height. Furthermore, each second-stage IC also integrates a precharge circuit for the flying-capacitor and output nodes to limit startup inrush current before normal switching operation begins.

Future work will proceed in three directions. First, the design will be validated through measurements after the chip fabrication. Second, an actual load IC will be designed and stacked above the interposer to measure the performance of the complete VPD system. Finally, a parallel architecture that aggregates multiple proposed converter modules will be developed and evaluated together with thermal and cooling analysis to extend scalability toward higher output-current applications.

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